EXTRA:
Exploiting eXascale Technology with Reconfigurable Architectures

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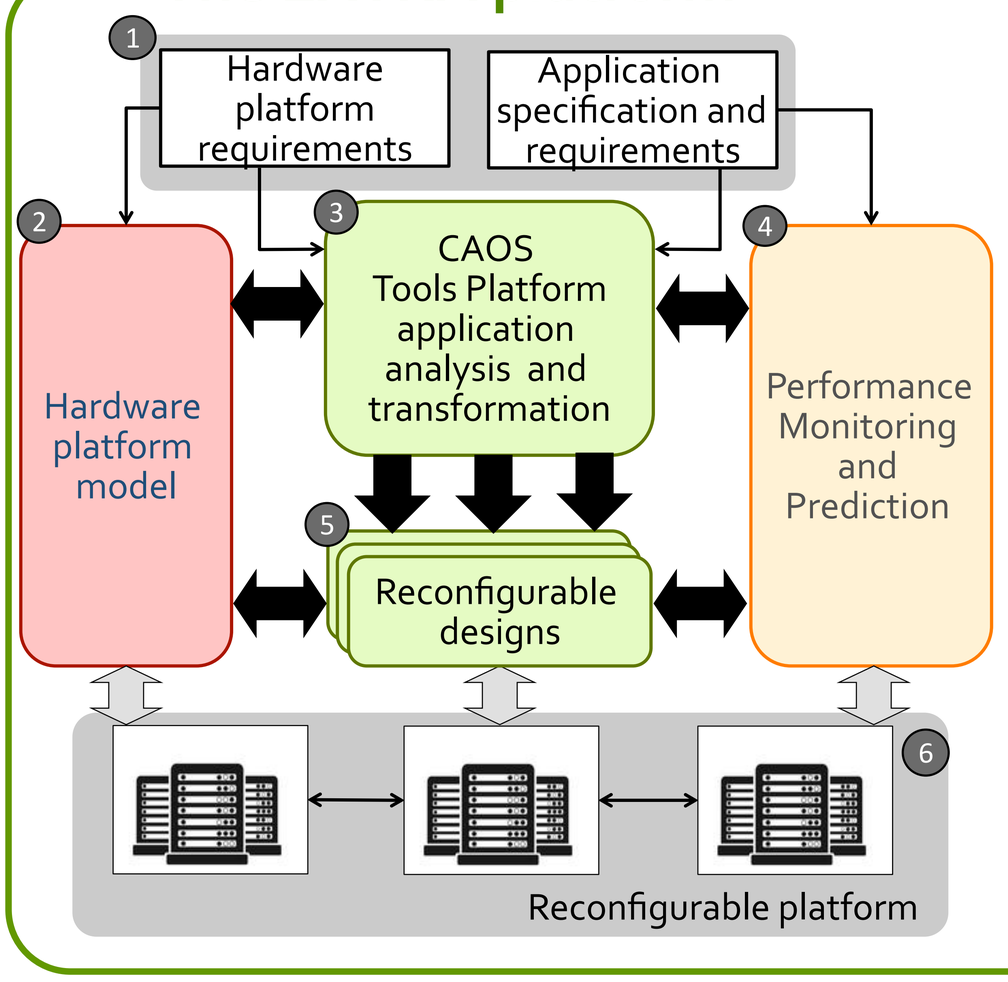
Mission statement

Create a flexible exploration platform for the development and optimization of architectures, tools, and applications targeting the next generation of exascale HPC systems using reconfigurable technology.

Research challenges

- Platform design and development for reconfigurable acceleration.
- Tool design for fast prototyping and design space exploration.
- Automated generation and deployment of reconfigurable kernels & applications.
- HPC application prototyping, performance analysis, modeling, and extrapolation.

The EXTRA platform



1 Information about the application and the target platform.

2 A hardware platform model that acts as target.

3 The CAOS Tools Platform generates a (set of) reconfigurable design(s).

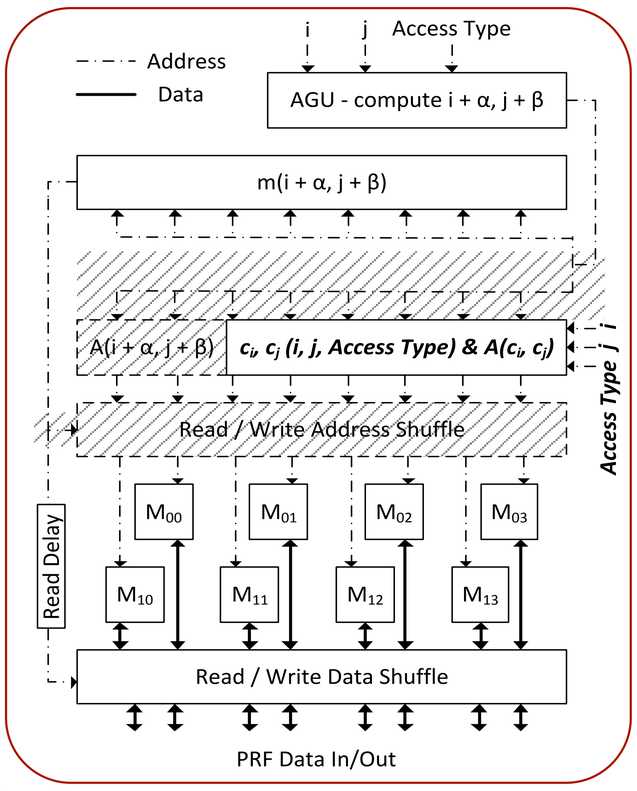
4 The Performance Monitoring and Prediction enables performance-centric design.

5 Candidate reconfigurable designs to select from for implementation.

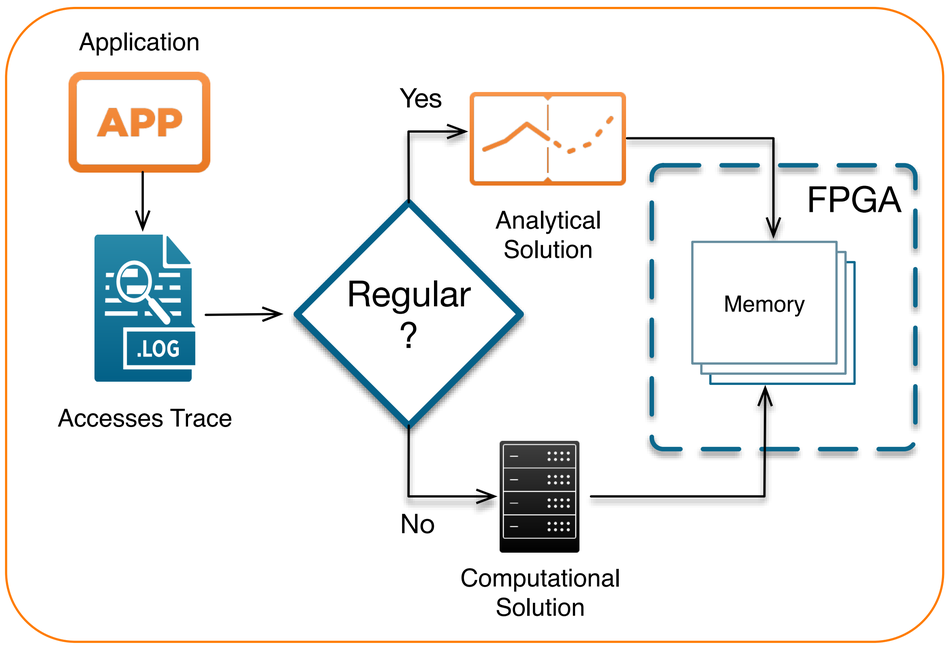
6 The Reconfigurable Platform corresponds to the hardware architecture and runtime of the reconfigurable HPC system.

@UvA: Parallel Memory Systems

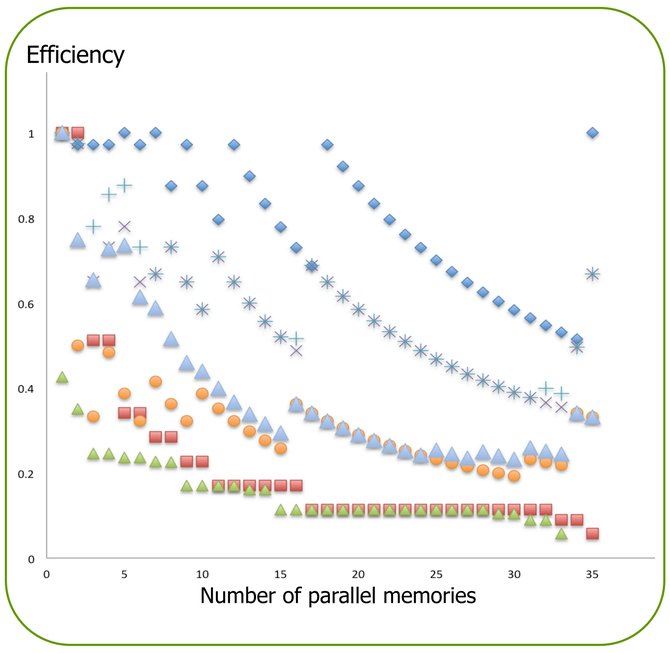
Design customizable parallel memory architectures.



Embedding parallel memory systems In hardware accelerators.



Modeling application-centric parallel memory efficiency.



More info...

[1] C.B.Ciobanu, G.Stramondo, A.L.Varbanescu. **Customizable Memory Systems for High Performance Reconfigurable Architectures**. In *HiPEAC ACACES'16*.

[2] D. Stroobandt, A. L. Varbanescu, C. B. Ciobanu, M. Al Kadi, A. Brokalakis, G. Charitopoulos, T. Todman, X. Niu, D. Pnevmatikatos, A. Kulkarni, E. Vansteenkiste, W. Luk, M. D. Santambrogio, D. Sciuto, M. Huebner, T. Becker, G. Gaydadjiev, A. Nikitakis and A. J. Thom, **EXTRA: Towards the exploitation of eXascale technology for reconfigurable architectures.** In *Reconfigurable Communication-centric Systems-on-Chip*, 2016.

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EXTRA

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Partners

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